Remarks/Arguments

There are no amendments to the specification, claims or the drawings herein.

In the claims, Claims 1-25 remain and are pending in the application. Claims 12-20 are allowed. Claims 1-8, 11 and 21-25 are rejected and Claims 9 and 10 are objected to. Reconsideration is respectfully requested.

The Examiner rejected Claims 1, 3-8, 11 and 21-25 under 35 U.S.C. 102(b) as being anticipated by Patel et al., U.S. Patent No. 6,025,737 (hereinafter 'Patel et al.').

Applicant respectfully traverses the rejection of Claims 1, 3-8, 11 and 21-25 in view of Patel et al. on the grounds that that the Examiner failed to establish a *prima facie* case of anticipation with respect to Patel et al. In particular, the Examiner has failed to establish that Patel et al. disclose, explicitly or implicitly, "each element of the claim under consideration" (*W.L. Gore & Associates v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983)) and failed to show that Patel et al. disclose the claimed elements "arranged as in the claim" (*Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)) as required by the Federal Circuit for *prima facie* anticipation under 35 U.S.C. 102.

Patel et al. generally disclose circuitry for a low internal voltage integrated circuit and more particularly, "[a] technique and circuitry for interfacing an integrated circuit manufactured using technology compatible with one voltage level to other integrated circuits compatible with a different voltage level" (Patel et al., Abstract, lines 1-4). Integral to the circuitry disclosed by Patel et al. is an input buffer using an inverter circuit configuration comprising transistor 1050 and transistor 1055, "coupled in series between a positive supply and ground" that is illustrated in Figure 10B (Patel et al., Col. 15, lines 13-14). In Figure 10C and at Col. 15, lines 48-50, which are relied upon by the Examiner, Patel et al. disclose, "an example of an implementation of the input buffer in FIG. 10B using programmable metal options, such as by selecting an appropriate metal mask". Patel et al. further disclose, "[t]he effective size (or strength) of transistor 1050 may be adjusted using transistors 1060 and 1062 ... the effective size (or strength) of transistor 1055 may be adjusted using transistors 1064 and 1066" (Patel et al., Col. 15, lines 50-54, further relied upon by the

Examiner). An embodiment of the disclosed adjustment employs "programmable metal options".

However, contrary to the Examiner's contention, Patel et al. fail to disclose, explicitly or implicitly, each element of at least Applicant's base Claim 1. For example, Patel et al. do not disclose a "bias generator" or an output thereof, as defined by Applicant's specification and recited in Applicant's Claim 1 (for example, see at least Applicant's specification, Page 5, line 28, through Page 6, line 9). Instead, in Figures 10B and 10C (relied upon by the Examiner), Patel et al. disclose an inverting input buffer (a.k.a. "inverter"). The disclosed inverting input buffer is not equivalent to Applicant's claimed bias generator and one skilled in the art would not consider them the same.

For example, as illustrated, the inverting input buffer receives a ***binary*** logic signal at I/O pin 820 from which an inverted ***binary*** logic output signal is produced at output 1058, labeled "To Core". The skilled artisan would recognize that the output binary logic signal has two ***and only two*** defined allowed values or states (e.g., logic voltages) dependent only on the supply voltages VCCQ or VCCINT and VSSQ during normal operation of the inverter. As such, the inverting input buffer of Figures 10B and 10C disclosed by Patel et al. cannot be the bias generator claimed by Applicant. In particular, the inverting buffer of Patel et al. is incapable of, "producing as an output signal a bias voltage V_{bias}" having "a magnitude that is selectable from among a set of available magnitudes,", as defined by Applicant for the bias generator recited in Applicant's claims (Applicant's specification, Page 5, line 30, through Page 6, line 1). Except for the metal programmability, the inverting input buffer disclosed by Patel et al. is a conventional buffer known in the art and entirely unrelated to the bias generator recited in Applicant's Claim 1.

Further, Patel et al. do not disclose, "means for adjusting a set of available magnitudes of a bias voltage output signal at the output using metal programming", as recited, in part, in Applicant's Claim 1. In particular, according to Patel et al. at Col. 15, lines 28-29, "the input threshold trip point of the inverter may be programmable" (i.e., using "metal options" associated with transistors 1060, 1062, 1064, and 1066) also see Col. 15, lines 48-53. As employed by Patel et al., "trip point of the inverter"

has its normal and customary meaning in the art (i.e., a voltage level at the I/O pin 820 at which the binary logic output signal at 1058 transitions from one logic level to another). At Col. 15, lines 29-31, Patel et al. further disclose, "[t]he input threshold trip point depends on the ratio of the relative ***strengths*** of the ratio of the pull-up transistor 1050 to the pull-down transistor 1055" (***emphasis*** added). According to Patel et al., "[t]he effective size (or strength) of transistor 1050 may be adjusted by using transistors 1060 and 1062," while "the effective size (or strengths) of transistor 1055 may be adjusted using transistors 1064 and 1066" (Patel et al., Col. 15, lines 50-54). As such, Patel et al. disclose programming the input ***threshold trip point*** of the inverter. In other words, Patel et al. disclose adjusting when, in a logic transition of an input signal, the input buffer output transitions from one logic level to another. However, the input threshold trip point has ***no effect*** on an output voltage produced by the inverter. Specifically, the adjustment disclosed by Patel et al. does not change or adjust a voltage of either or both of the two logic levels produced by the buffer at an output. Thus, Patel et al. clearly do not disclose, "means for adjusting a set of available magnitudes of a bias voltage ***output*** signal," as claimed by Applicant.

Moreover, the Examiner is respectfully incorrect that at Col. 7, lines 55-60, "Patel et al. discloses a bias generator [1050, 1055] for testing (intended of use) of a static random access memory SRAM". In fact, at Col. 7, lines 55-60, Patel et al. merely disclose, "[t]here are many techniques for implementing the programmable options feature of the present invention ..." and specifically mentions that the programmable options, "include, and are not limited to, laser programmable options, fuses, antifuses, ... EEPROM, Flash EPROM, and SRAM, and many others". However, neither at Col. 7, lines 55-60, nor anywhere else therein do Patel et al. disclose or even suggest "a bias generator for testing a static random access memory (SRAM)". In fact, Patel et al. never even disclose or suggest testing SRAM using any other circuit. The word 'test' or its many art-recognized variants never appears in the disclosure of Patel et al. Thus, the Examiner respectfully cannot properly contend that Patel et al. discloses or even suggest a bias generator for testing SRAM.

Regarding Applicant's base Claim 6, Patel et al. fail to disclose all of the elements recited therein. For example, Patel et al. at least fail to disclose, "a metal-programmable transistor that adjusts a set of available magnitudes of a bias voltage

output signal at the bias generator output when metal programmed", as recited in Applicant's Claim 6. As discussed above with respect to Claim 1, Patel et al. disclose metal options for adjusting an ***input threshold trip point*** of an inverting input buffer. However, the input threshold trip point does not affect an output voltage of the buffer. As such, the Examiner is respectfully incorrect in contending that the metal options associated with the programmable input threshold trip point of Patel et al. are, or reasonably could be, the claimed, "metal-programmable transistor that adjusts a set of available magnitudes of a bias voltage output signal," as recited in Applicant's Claim 6. In addition, as discussed with respect to Claim 1 above, Patel et al. fail to disclose, at least, "a bias generator", and "testing of a static random access memory (SRAM)", as is further recited in Applicant's Claim 6.

Regarding Applicant's base Claim 21, Patel et al. fail to disclose all of the elements recited therein, contrary to the Examiner's contention. In addition to those elements discussed above with respect to Applicant's Claims 1 and 6, Patel et al. at least fail to disclose, "providing a metal-programmable transistor in the bias generator," as well as, "metal programming ... to modify the available magnitudes of the set", as recited in Applicant's Claim 21. In particular, the provided metal-programmable transistor must be ***in*** the bias generator, as claimed in Claim 21. Patel et al. do not disclose a bias generator. Further, Patel et al. fail to disclose any means including a metal programmable transistor that modifies the available magnitudes of the set of voltages produced by the bias generator. The metal options disclosed by Patel et al. specifically adjust an input trip point and not an output voltage of the disclosed input buffer. In short, Patel et al. fail to disclose or even suggest a "method of modifying a set of available magnitudes of a bias voltage output signal generated by a bias generator", as recited in Applicant's base Claim 21.

Therefore, Applicant respectfully submits that the Examiner failed to establish separately for each of Applicant's base Claims 1, 6 and 21 a *prima facie* case of anticipation with respect to Patel et al. In short, Patel et al. clearly fail to disclose, "each element of the claim under consideration" (*W.L. Gore & Associates v. Garlock*, cited *supra*) when considering Applicant's base Claims 1, 6 and 21. In particular, as detailed above, the Examiner failed to show that there is, "no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary

skill in the field of the invention," as required by the Federal Circuit. *Scripps Clinic & Research Found. V. Genentech Inc.*, 927 F.2d 1565, 18 USPQ 2d 1001, 1010 (Fed. Cir. 1991).

Having failed to establish *prima facie* anticipation of base Claims 1, 6 and 21, the Examiner similarly failed to show that dependent Claims 3-5, 7-8, 11, and 22-25 are *prima facie* anticipated by Patel et al. In particular, Claims 3-5 are dependent from and include all of the limitations of base Claim 1; Claims 7-8 and 11 are dependent from and include all of the limitations of base Claim 6; and Claims 22-25 are dependent from and include all of the limitations of base Claim 21. Hence, the rejection of base Claims 1, 6 and 21, as well as dependent Claims 3-8, 11 and 22-25, under 35 U.S.C. 102(b) is unsupported by facts in evidence and must be withdrawn.

The Examiner rejected Claim 2 under 35 U.S.C. 103(a) as being unpatentable by Patel et al. further in view of Ando, U.S. Patent No., 6,560,142 (hereinafter 'Ando'). The Examiner admitted, "Patel et al. ... does not discloses [*sic*] the bias output signal (To Core) is biases [*sic*] a gate of a weak write pull-down transistor of a write drives [*sic*] in the memory (SRAM)". The Examiner contended, "Fig 1 of Ando discloses a bias signal (WW) is biasing a gate of a weak write pull down transistor (1) of a writer [*sic*] driver (WB) in the memory". The Examiner concluded, "it is obvious to use the bias generator of Patel et al. in an environment where a driver of a memory is needed or a general combination of memory system elements to provide a particular end result". The Examiner further suggested, "[o]ne a [*sic*] particular end result is know [*sic*] from the viewpoint of overall memory system," and stated, "it would be obvious to use the particular circuit with specifics [*sic*] components as discussed in Ando to meet refinement for that specific use". The Examiner contended, "refinement of know [*sic*] circuitry such as that taught in Ando is ***well known*** in the operating and use of memory circuitry ... and is considered to be routine part of the final stages prior to final preparation for sale and end use" (***emphasis*** added). The Examiner's contention regarding the "well known" nature of refinement was made without providing extrinsic evidence in support of the contention.

Applicant respectfully traverses the rejection under 35 U.S.C. 103(a) on the grounds that the Examiner failed to establish and properly support a *prima facie* case

of obviousness with respect to Patel et al. in view of Ando (hereinafter 'the references'). Specifically, the Examiner did not show, with respect to the rejected claim, one or more of 1) "some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings"; 2) "a reasonable expectation of success" in modifying or combining the teachings of the references; and 3) that the prior art references "teach or suggest all the claim limitations", as required by the courts. MPEP, Section 2142, *Establishing a Prima Facie Case of Obviousness*. Moreover, the Examiner failed to establish that the teaching or suggestion to make the claimed combination and the reasonable expectation of success are both "found in the prior art, and **not** based on applicant's disclosure". *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991) (***emphasis*** added). In short, the Examiner's reasons for rejecting Claim 2 respectfully fail to meet even the minimum requirements necessary for establishing and maintaining *prima facie* obviousness with respect to the references.

As is clearly stated in the MPEP, "[o]bviousness can ***only*** be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation ***to do so*** found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art" (***emphasis*** added). MPEP §2143.01 *Suggestion or Motivation to Modify the References.* Additionally, according to the Federal Circuit, " 'teachings of references can be combined only if there is some suggestion or incentive to do so' "(emphasis in original). *In re Fine*, 837, F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (quoting *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). "[E]ven when the level of skill in the art is high, the Board [or the Examiner] must identify specifically the principle, known to one of ordinary skill, ***which suggests the claimed combination***. In other words, the Board [or the Examiner] must ***explain the reasons*** one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious" (***emphasis*** added). *In re Rouffet*, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998).

Thus, a motivation to combine is an ***essential element*** in establishing *prima facie* obviousness. For a motivation to be legitimate, there ***must be a finding*** that a 'teaching, suggestion, or motivation' to combine ***exists***. There ***must be objective evidence of record*** from the prior art in light of the motivation both to support the Examiner's selection of the particular references and to support combining the elements or teachings thereof, as proposed by the Examiner. The Examiner ***is required*** by way of reasoned explanation ***to specifically identify the principle*** known by the skilled artisan '***that suggests the claimed combination***'. The Examiner may not simply dispense with providing such evidence and reasoning in presenting the motivation to combine.

Moreover, "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art ***also suggests the desirability*** of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)" (***emphasis*** added). MPEP §2143.01, cited *supra*. For a motivation to combine/modify to be legitimate and therefore, be employed to support a *prima facie* case of obviousness, there must be "evidence that 'a skilled artisan, ***confronted with the same problems as the inventor*** and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed'". *Ecolochem, Inc. v. Southern Calif. Edison Co.*, 227 F.3d 1361, 1375, 56 USPQ2d 1065, 1075 (Fed. Cir. 2000) (quoting *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1456 (Fed. Cir. 1998)) (***emphasis is*** added). Therefore, in addition to providing evidence from the prior art to support selecting and combining, the Examiner is ***required*** to establish and provide ***evidence*** to support the ***desirability*** of the combination in light of the ***problem or problems*** that faced ***the inventor***.

Regarding Patel et al. and Ando, the Examiner merely states without ***evidentiary support*** that it would be obvious to combine the references based on what appears to be a hypothetical rationale that the Examiner considered 'routine'. However, the Examiner has not and respectfully cannot point to any portion of the respective disclosures of Patel et al. or Ando where such a motivation is explicitly expressed. Thus, the Examiner's motivation to combine/modify the references is clearly not found 'in the references themselves'.

Furthermore, the Examiner provided ***no extrinsic evidence to support*** a contention that a teaching, suggestion, or motivation ***not found explicitly*** in the cited references was ***either present implicitly*** in that taught by the references (which in this instance, clearly it is not) ***or*** was ***in the knowledge generally available to one of ordinary skill in the art***. Specifically, ***the Examiner cited nothing*** (i.e., no extrinsic evidence) beyond the references themselves in support of the Examiner's motivation. Therefore, the Examiner ***is not*** relying on implicit teachings or general knowledge of the skilled artisan. As such, the Examiner respectfully cannot contend that the Examiner's motivation regarding combining the references are "found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art", as required by the courts to support *prima facie* obviousness. *In re Kotzab,* 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

In addition, the Examiner's motivation lacks that necessary to qualify as a legitimate or supported motivation to combine/modify according to the courts. In particular, the Examiner offered no explanation regarding how the proposed motivation would lead the skilled artisan to select and combine the references, as relied upon by the Examiner for the subject rejection. No explanation is presented regarding "the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them [thereby rendering] the claimed invention obvious". *In re Rouffet*, cited *supra*. In short, the Examiner's motivation fails to address ***why*** a skilled artisan, ***without*** knowledge or benefit of Applicant's teachings, would make the ***specific choice*** to combine Patel et al. and Ando as opposed to some other combination of references.

In addition, the Examiner's motivation provides no insight into why one skilled in the art would have found it obvious to make the particular and specific modification of the relevant teachings of references that the Examiner suggests other than a vague and unsupported statement that it is "well known in operating and use of memory circuitry". Thus, the Examiner's motivation fails to address why the skilled artisan would have been motivated to combine/modify Patel et al. and Ando.

Additionally, the Examiner failed to establish, or for that matter, even attempt to establish, that the prior art or the skilled artisan with ***no knowledge of the claimed invention*** would have: (a) recognized the desirability of the combination/modification proposed by the Examiner, or (b) selected the specific elements from the cited prior art references for combination/modification, as suggested by the Examiner, when confronted with the same problem faced by the inventor. In fact, the Examiner did not explicitly or implicitly consider the problem(s) faced by the inventor as motivation for the combination/modification proposed by the Examiner. Similarly, the Examiner has not identified specifically the principle of or explained the reasons why the skilled artisan would have been motivated to select and combine the references. *In re Rouffet*, cited *supra*. Hence, the Examiner simply has not provided a legitimate motivation to combine the cited references in support of a *prima facie* case of obviousness.

An absence of a legitimate or supported motivation to combine Patel et al. and Ando defeats a *prima facie* case of obviousness with respect to Claim 2. Furthermore, given the lack of a supported motivation to combine the respective references, any consideration regarding what the respective combination might or might not disclose is rendered moot.

Notwithstanding the lack of a supported motivation to combine/modify, the combination of Patel et al. and Ando also fails to disclose or suggest ***all*** of the claim limitations of Claim 2. In particular, the combination of the references fails to disclose or suggest all of the limitations recited separately in at least Applicant's base Claim 1. For example, Patel et al. combined with Ando at least fail to disclose one or more of a "bias generator", "an output of the bias generator" and "means for adjusting a set of available magnitudes of a bias voltage output signal at the output using metal programming". Claim 2 is dependent from and includes all of the limitations of Claim 1.

In addition, the combination of Patel et al. and Ando further fail to disclose, "wherein the bias voltage output signal biases a gate of a weak write pull-down transistor of a write driver in the SRAM with a target magnitude predetermined for the SRAM". For example, neither Patel et al. nor Ando disclose or suggest, "a weak

write pull-down transistor", as claimed by Applicant. Furthermore, the reference to "WW" in Ando is to a "write word signal" (Col. 3, lines 10-11). Such a 'write word signal' is unrelated to "the bias voltage output signal" that "biases a gate of a weak write pull-down transistor of a write driver ...", as claimed in Applicant's Claim 2. Moreover, neither Patel et al. nor Ando, whether considered separately or together, mentions or suggests a "write driver in the SRAM" or that there may be "a target magnitude [of the bias] predetermined for the SRAM", as claimed in Claim 2. In fact, the disclosure of Ando is entirely directed to a capacitorless DRAM gain cell and does not even mention or consider SRAM.

As such, contrary to the Examiner's contention, the combination of Patel et al. and Ando fails to disclose or suggest all of the limitations of Claim 2, as required by the courts for establishing and supporting *prima facie* obviousness. See *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). As with a failure to provide a legitimate motivation to combine, a failure by the combined references to disclose or suggest all of the limitations of Claim 2 further defeats *prima facie* obviousness. *In re Royka*, cited *supra*.

At least for the reasons set forth above, the Examiner's rejection under 35 U.S.C. 103(a) lacks proper support for a *prima facie* case of obviousness according to the case law. Thus, the rejection of Claim 2 under 35 U.S.C. 103(a) by Patel et al. in view of Ando must be withdrawn.

Applicant appreciates the Examiner's acknowledgement of the allowability of Claims 9 and 10 if rewritten in independent form. However, in light of Applicant's remarks above, Applicant respectfully submits that Claims 9 and 10 are in allowable form, as originally filed. Applicant respectfully declines to rewrite these claims pending the Examiner's consideration of the remarks presented hereinabove for the respective base claim.

In addition, Applicant appreciates the Examiner's allowance of Claims 12-20, as filed.

In summary, Claims 1-25 were pending. Claims 12-20 were allowed, Claims 1-8, 11 and 21-25 were rejected, and Claims 9 and 10 were objected to. It is

respectfully requested that Claims 1-11 and 21-25 be allowed along with allowed Claims 12-20, and that the application be passed to issue at an early date.

Should the Examiner's action be other than allowance, the undersigned respectfully requests a telephone call from the Examiner to discuss further consideration that would expedite the prosecution of the application. Furthermore, should the Examiner have any questions regarding the above, please contact the undersigned, J. Michael Johnson, Agent for Applicant, at telephone number (775) 849-3085.

Respectfully submitted,
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